

**Tender No: C-DACB/R&D/PCB-Tool/11-12**

**Date: 03.12.2011**

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**CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING  
(C-DAC)**

**(A Scientific Society under the Department of Information Technology,  
Ministry of Communications and IT, Govt. of India)  
No.1, CDAC Knowledge Park, Old Madras Road,  
Byappanahalli, Bangalore-560038  
Ph: 080-66116400-03 Fax: 080-25247724**

**Ref No: C-DACB/R&D/PCB-Tool/11-12**

**December 03, 2011**

**TENDER NOTICE**

**Supply and Installation of PCB Design Tool suite with High Speed SI & PI  
simulation etc.,**

C-DAC, Bangalore (A Scientific Society under Ministry of Communications & Information Technology, Govt. of India) invites sealed tenders in Two-Bid system either from the Original Equipment Manufacturers (OEM) or their authorized Direct Distributors / Indian Agents towards supply and installation of “ PCB Design Tool suite with High Speed SI & PI simulation etc.”. Interested bidders may either download the detailed tender document from <http://www.cdacb.in/tenders> or collect it during 05-12-2011 to 22-12-2011 from our above mentioned address between 10.00 am and 5.00 pm on all working days and submit the same as per the given schedule in this tender document.

**Joint Director (Admin)**

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**TENDER SCHEDULE**

TENDER NO: C-DACB/R&D/PCB-Tool/11-12

Date of issue of Tender documents	December 03, 2011
Date of Pre-bid meeting	December 12,2011, 16.00 Hrs
Last date of submission of bids	December 23, 2011, 15.00 Hrs
Date of opening of Technical bids	December 23, 2011, 15.30 Hrs
Tender Fee (Non-Refundable)	Rs.1,000/- (Rupees One Thousand Only) in the form of Demand Draft favoring CDAC, payable at Bangalore. In case the documents are downloaded from the website, Demand Draft for an amount of Rs.1,000/- in favor of C-DAC, payable at Bangalore should be enclosed along with Technical Bid. Non submission of tender fee will render the tender as invalid and will be rejected outrightly.
Earnest Money Deposit	Rs.1,00,000/- (Rupees One Lakh Only) in the form of Demand Draft favoring C-DAC, payable at Bangalore
Date of Opening of Commercial Bids	Shall be notified later to the technically qualified bidders.

All the pages of tender document should be duly signed and stamped by the competent authority.

**SECTION I: INVITATION FOR BIDS (IFB)**

1. Centre for Development of Advanced Computing invites sealed bids for Supply & Installation of “PCB Design Tool suite with High Speed SI & PI simulation etc.,” at C-DAC Knowledge Park, Bangalore.

**2. Two Bid System :**

The two bid system will be followed for this tender. In this system bidders must submit their offer in two separate sealed envelopes as explained below

**• Envelope No.1: “Technical Bid” shall contain :**

- a) The Demand draft towards Earnest Money Deposit for **Rs.1,00,000/-**
- b) Duly filled Technical Bid with proper seal and signature of authorized person on each page of the bid submitted.
- c) The detailed Bill of Materials, technical specification, make & model of the tool and compliance to the Schedule of Requirement (Section IV) for which bid is submitted.
- d) The soft copy of Technical Bid (.doc / .xls format) in a CDR (except certificates, brochures, order copies etc.)
- e) Copy of the Un-Priced Commercial Bid with commercial terms and conditions as attached in the “Commercial Bid” without mentioning any price.

- f) Undertaking to the effect that a Security Deposit of 5% of the order value will be submitted in case C-DAC decides to place the Purchase Order.
- g) Other related documents as mentioned in the tender document but not listed here.

• **Envelope 2 : “Commercial Bid” shall contain:**

Price Schedule completed in all respects with proper seal and signature of the authorized person with the same commercial terms and conditions as submitted with technical bid.

Both the technical bid and commercial bid envelopes should be sealed separately and clearly marked as “Envelope No. 1 – Technical Bid” and “Envelope No. 2 – Commercial Bid” and addressed to:

**The Joint Director (Admin)**

**Centre for Development of Advanced Computing (C-DAC),**

**C-DAC Knowledge Park, No.1 Old Madras Road,**

**Byappanahalli, Bangalore – 560 038**

Please write the **tender number** on each envelope and seal all the envelopes.

**Note:** Please do not put “Commercial Bid” (prices quoted) in the technical bid envelope. If the price quoted is submitted with technical bid the tender will be rejected.

**3. Pre Bid Meeting:**

The Pre-bid meeting shall be held on December 12, 2011 at 1600 hrs at

**Centre for Development of Advanced Computing (C-DAC),**

**C-DAC Knowledge Park, No.1 Old Madras Road,**

**Byappanahalli,**

**Bangalore – 560 038**

The queries, if any, should be submitted in writing on/before the day of Pre-Bid meeting and the answers to the queries will be made available during meeting/website.

**No queries shall be entertained after the Pre-Bid Meeting.**

**4. Date of Submission of bids and opening of the technical bids.**

- Last date for submission of bids is December 23, 2011 up to 1500 hrs at

**Centre for Development of Advanced Computing (C-DAC),**

**C-DAC Knowledge Park, No.1 Old Madras Road,**

**Byappanahalli,**

**Bangalore – 560 038**

- Technical bid will be opened on December 23, 2011 at 15.30 Hrs.

The bid can be submitted in person or through post/courier (C-DAC shall not be responsible for any postal delays resulting in disqualification / rejection of any bid) so as to reach on or before the due date and time.

The representative(s) of bidders may choose to attend the opening of the technical bids. In case bidder requires any clarification / information they may contact C-DAC at the address mentioned above.

The technical bids will be evaluated to shortlist the eligible bidders. The technical bids of only the short listed eligible bidders shall be considered for technical evaluation.

Bidder whose technical bid is found to be acceptable and meeting the eligibility requirements as specified in this tender will be informed about the date and time of the opening of commercial bid.

## **5 Opening of Commercial Bid**

The Commercial bids of the short listed bidders only will be opened, in the presence of the bidders or their authorized representative, who choose to attend, at the time, place and date to be informed later.

The authorized representative of bidder, present at the time of opening of the bids shall be required to sign an attendance register as a proof of having attended the commercial bid opening.

The bidder's name, bid prices, discounts and such other details considered as appropriate by C-DAC, will be announced at the time of opening of the bids.

**(Technically accepted competitive bids ONLY will be considered for the opening of Commercial Bids)**

**END OF SECTION I**

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**SECTION II: INSTRUCTION TO BIDDERS (ITB)**

**1. Delivery Period / Timelines**

The Supply & Installation at site must be completed within 8 weeks, after placement of Purchase order or opening of the LC, as the case may be.

**2. Location for the Supply, Installation & Maintenance Services.**

The PCB Design Tool suite with High Speed SI & PI simulation etc., covered by this document are required to be supplied and installed at C-DAC, CDAC Knowledge Park, Bangalore-560038.

**3. Order Placement and Release of Payment**

The Purchase Order and payment shall be processed by:

**Centre for Development of Advanced Computing (C-DAC),  
C-DAC Knowledge Park, No.1 Old Madras Road,  
Byappanahalli,  
Bangalore – 560 038**

**4. Eligible Bidders:**

1.1 The bidder should be either a principle manufacturer or authorized distributor/reseller for all the items as mentioned in the tender document.

1.2 Bidders should not be under a declaration of ineligibility for **corrupt and fraudulent** practices.

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- 1.3 Bidders should be registered with Sales Tax / Income Tax Department of Government of India and should hold a valid VAT registration certificate, as applicable.
  - 1.4 The bidder should submit the relevant and necessary documents along with the technical bid.
  - 1.5 The Bidder should have the main / branch office at Bangalore to ensure satisfactory after sales service support.

**Note: C-DAC reserves the right to award/reject the orders to any particular bidder without assigning any reasons thereof.**

#### **5. Amendment to Bidding Documents:**

- 5.1 At any time prior to the deadline for submission of bids, C-DAC may, for any reason, whether on its own initiative or in response to the clarification request by a prospective bidder, modify the bid document.
- 5.2 The amendments, if any, will be notified in writing to the bidders and such amendments/modifications will be binding on bidders.
- 5.3 C-DAC at its discretion may extend the deadline for the submission of bids if the bid document undergoes changes during the bidding period, in order to give prospective bidders time to incorporate the amendments while preparing the bids.

#### **6. PREPARATION OF BIDS:**

Bidders should avoid, as far as possible, corrections, overwriting, erasures or postscripts in the bid documents. In case however any corrections,

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alterations, changes, erasures, amendments and/or addition have to be made in the bids, they should be supported by dated signatures of the same authorized person signing the bid documents.

## **7. Earnest Money Deposit (EMD)**

7.1 The tender documents must be accompanied by Earnest Money Deposit of Rs.1,00,000/- (Rupees One Lakh only) in the form of Demand Draft (DD) drawn in favour of C-DAC payable at Bangalore.

Bids submitted without EMD will stand rejected. EMD will not be accepted in the form of cash/cheque/FDR/BG or any other form except DD. No interest shall be payable on EMD.

7.2 The EMD will be returned to the bidder(s) whose offer is not accepted by C-DAC within 30 days from the date of opening of commercial bids. In case of the bidder(s) whose offer is accepted, the EMD will be returned on submission of Security Deposit (Refer clause 4 of Section III). However, if the return of EMD is delayed for any reason, no interest/penalty shall be payable to the bidder.

7.3 The successful bidder, on award of contract / order must send the contract / order acceptance in writing within 10 days of award of contract/order, failing which the EMD will be forfeited and the order will be placed on the next successful bidder.

7.4 The EMD shall be forfeited:

7.4.1 If the bidder withdraws the bid during the period of bid validity specified in the tender.

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7.4.2 In case a successful bidder, fails to furnish the security deposit  
(Refer clause 4 of Section III)

7.4.3 If the bidder fails to furnish the acceptance in writing, within 10  
days of award of contract/order.

## **8. Period of validity of bids:**

**8.1** Bids shall be valid for a minimum 120 days from the date of submission.  
A bid valid for a shorter period shall stand rejected.

**8.2** C-DAC may ask for the bidder's consent to extend the period of validity.  
Such request and the response shall be made in writing only. The bidder is  
free not to accept such request without forfeiting EMD. A bidder agreeing  
to the request for extension will not be permitted to modify his bid.

## **9. SUBMISSION OF BIDS**

The bid should be neatly arranged, pages numbered and secured properly.  
Each page of the bid should be signed by the authorized representative.  
They should not contain any terms and conditions, printed or otherwise,  
which are not applicable to the bid. The conditional bid will be summarily  
rejected. Insertions, postscripts, additions and alterations shall not be  
recognized, unless confirmed by bidder's signature.

## **10. Deadline for Submission of Bids:**

10.1 Bids must be received by C-DAC before the due date and time at the  
address specified in the tender document. In the event of the specified date  
for the submission of bids being declared as a holiday for C-DAC, the bid-  
closing deadline will stand extended to the next working day up to the  
same time.

10.2 C-DAC may extend this deadline for submission of bids by amending the bid document and the same shall be suitably notified to the bidders.

**11. Late Bids:**

Any bid inadvertently received by C-DAC after the deadline for submission of bids, will not be accepted and returned unopened to the bidder.

**12. BID OPENING AND EVALUATION OF BIDS****Opening of Bids:**

12.1 The technical bids will be evaluated to shortlist the eligible bidders. The technical bids of only the eligible bidders shall be considered for further processing (Technical evaluation).

12.2 During the evaluation process, C-DAC may seek clarification from the bidder, if required. The bidder may submit clarification as required and / or submit the documents, catalogs, literature etc., in response to the clarifications. However, any changes in make/model quoted, quantity offered, configuration, capacity, speed etc., will not be permitted.

12.3 Bidder whose technical bid is found to be acceptable and meeting the eligibility requirements as specified in this tender will be informed about the date and time of the opening of the commercial bid.

12.4 C-DAC will open commercial bids of only the technically short listed bids, in the presence of the bidder or their authorized representative who choose to attend the bid opening, at the time and date to be informed later.

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12.5 The bidder's authorized representative who attends the bid opening shall sign an attendance register as a proof of having attended the bid opening.

12.6 The bidder's name, bid prices, discounts and such other details considered as appropriate by C-DAC, will be announced at the time of opening of the commercial bids.

### **13. Comparison of Bids:**

13.1 Only the short-listed bids from the technical evaluation shall be considered for commercial comparison.

13.2 The Schedule of Requirements stipulates the requirements and features/modules only and is not complete Bill of Materials. The commercial comparison will include all such features/modules that are required to achieve the requirements. Bidders, in their own interest, should quote for all the features/modules essential for this purpose.

13.3 The prices for the complete solution (all essential features/modules put together) only will be compared.

13.4 For the purpose of comparison, the exchange rate as on the date of opening of commercial bids will be considered.

13.5 The comparative statement shall also indicate the delivery schedule offered in the technical bid. The bid not adhering to the delivery/installation period as mentioned in Clause 1 of Section II will stand rejected.

## **14. AWARD OF CONTRACT**

### **Award Criteria**

- 14.1 C-DAC shall award the contract to the eligible bidder whose technical bid has been accepted and determined as the lowest evaluated commercial bid.
- 14.2 If more than one bidder happens to quote the same lowest price, C-DAC reserves the right to split the order and award the contract to more than one bidder.

## **15. Purchaser's Right to amend / cancel**

- 15.1 If, for any unforeseen reasons, C-DAC is required to change/reduce the Scope of Supply, this change shall be acceptable to the bidder without change in the unit price quoted.
- 15.2 C-DAC reserves the right to cancel the tender without assigning any reasons there for.

## **16. Corrupt or Fraudulent Practices.**

- 16.1 It is expected that the bidders who wish to bid for this project have highest standards of ethics.
- 16.2 C-DAC will reject bid if it is revealed that the bidder has engaged in corrupt and / or fraudulent practices while competing for this contract
- 16.3 C-DAC may also declare a bidder ineligible, either indefinitely or for a stated duration, for participating in C-DAC's tender process, if it is revealed that the bidder has engaged in corrupt and / or fraudulent practices while competing for this contract.

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**17. Interpretation of the clauses in the Tender Document / Contract Document:**

In case of any ambiguity / dispute in the interpretation of any of the clauses in this tender document, interpretation of Executive Director, CDAC, CDAC-KP, Bangalore shall be final and binding on all parties.

**END OF SECTION II**

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**SECTION III: SPECIAL CONDITIONS OF CONTRACT (SCC)****1. Prices**

- 1.1 The prices quoted shall be considered firm and no price escalation will be permitted during the validity of the bids.
- 1.2 Bidder may bid in Foreign Currencies or in INR. If bidder chooses to bid in foreign currency, the bidder must provide the name and address of the supplier abroad on whom the purchase order is to be placed. The LC would be opened, if applicable, favoring the same supplier abroad. The payment in foreign currency shall be made only if the order and LC is in the name of supplier abroad.
- 1.3 The prices quoted should be inclusive of freight, insurance & packing till C-DAC, Bangalore. The packing shall be transport worthy so as to prevent their damage or deterioration to goods during transit to their final destination.

**2. Taxes and Duties:**

- 2.1 The prices quoted should be inclusive of applicable taxes and duties, except customs duty and/or Central Excise Duty, as applicable. The items being imported in India are exempted from payment of Customs duty under Customs Notification No. 51/96 as amended by 24/2007, dated 1.3.2007. The Customs Duty Exemption Certificate shall be arranged by C-DAC as & when required. The Excise Duty exemption certificate will be issued under Notification No. 16/2007-Central Excise, dated 1.3.2007. The Customs duty payable after availing exemption, will be extra at actual.
- 2.2 In case of Import, Bidder shall arrange to clear the consignment after following customs formalities at port of landing in India and arrange to

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deliver the consignment to C-DAC, Bangalore. The cost and risk of the consignment rests with the bidder till it is delivered to C-DAC Bangalore.

- 2.3 If the taxes and duties are quoted separately, the exact rates and amounts of taxes should be mentioned. No concessional tax form (C/D) will be given by C-DAC.

### **3. Software Licenses:**

The Software tool mentioned in Schedule of Requirement is for Government R & D purpose only. The bidder must quote for Floating licenses. All the licenses must be perpetual. The software licenses shall be required in the name of C-DAC.

### **4. Security Deposit (SD)**

The successful bidder will be required to furnish the Security Deposit for 5% of the order value within 10 days of receipt of Purchase Order. The Security Deposit will be in INR and shall be submitted in the form of Demand Draft drawn in favor of C-DAC payable at Bangalore. The Security Deposit will be returned upon completion of installation & commissioning and submission of Performance Bank Guarantee (PBG). The Security deposit from the Indian representative is acceptable.

### **5. Performance Bank Guarantee (PBG)**

The successful bidder will be required to furnish the Performance Bank Guarantee for the 10% amount of the Purchase Order, as per the format attached to this document (Refer Annexure – B) on successful installation & commissioning of PCB Design Tool suite with High Speed SI & PI simulation etc.,. This bank guarantee shall remain valid for the entire period of maintenance of 3 years. This Performance Bank Guarantee must be in INR, issued by any Indian bank only.

## **6. Completeness Responsibility**

Notwithstanding the scope of work, engineering, supply and services stated in bid document, any equipment or material, engineering or technical services which might not be even specifically mentioned under the scope of supply of the vendor and which are not expressly excluded there from but which are necessary for the performance of the PCB Design Tool suite with High Speed SI & PI simulation etc., in accordance with the specifications and executing the contract to establish achievement of performance guarantee parameters, are to be provided for and rendered by the vendor without any extra charge.

## **7. Maintenance & Support**

All the tools offered / ordered, shall carry minimum 3 (three) years on site comprehensive maintenance & Support from the date of acceptance. The maintenance and support should be provided by OEM. The repairing/ rectification/ replacement/ configuration required, if any, of the software tools under maintenance must be done at site only at free of charge, including to and fro transportation costs of the items.

During the maintenance, all complaints should be rectified within 48 hours from the time of complaint. Beyond 48 hours, an equivalent or better standby will have to be provided within 72 hours from the time of complaint. Failure to do so would result in the invoking of the PBG. The PBG will be released only after the submission of satisfactory performance certificate issued by C-DAC after the completion of maintenance period.

**8. Payments:**

**In case of orders in INR** - 90% of the payment will be made against successful installation & commissioning of the software tool duly certified by C-DAC.

Balance 10% payment will be made on the completion of maintenance period OR against submission of Bank Guarantee of equivalent amount from any Indian bank valid for the entire period of maintenance of 3 years.

**In case of orders in foreign currencies** – 90% Payment shall be made against irrevocable Letter of Credit (LC) at sight. The balance 10% payment will be made by sight draft and shall be paid against submission of Performance Bank Guarantee as per clause 5 of Section III given above. In case of foreign bidder, the Performance Bank Guarantee submitted by bidder's Indian office/ representative/ distributor will be acceptable.

**9. Training:**

The Bidder should provide training covering all tools and other supplied software for a group of 10 people, 5 times ( total 25 days) spread over first two years of maintenance period as per vendor and CDAC's mutual date of convenience. The training could be arranged at CDAC, Bangalore or at vendor's place.

**10. Documentation:**

Complete legal documentation of all tools and other supplied software should be provided.

**11. Penalty for delayed Deliveries / Services.**

C-DAC reserves the right to levy penalty @ of 0.5% of order value per week of delay beyond the scheduled deliveries / execution of the order successfully, subject to maximum of 10% of the order value.

C-DAC reserves the right to cancel the order in case the delay is more than 10 weeks.

The penalties, if any shall be recovered from Security Deposit / Performance Bank Guarantee.

**12. Responsibilities:**

In case the bid is submitted by Indian Representative or authorized distributor/ reseller, with the instruction to place the purchase order on their principles, all the terms and conditions stipulated in this document shall apply to the principles on whose name the Purchase Order is placed.

**13. Jurisdiction:**

The disputes, legal matters, court matters, if any shall be subject to Bangalore jurisdiction only.

**14. Force Majeure:**

C-DAC may consider relaxing the penalty and delivery requirements, as specified in this document, if and to the extent that, the delay in performance or other failure to perform its obligations under the contract is the result of a Force Majeure. Force Majeure is defined as an event of effect that cannot reasonably be anticipated such as acts of God (like earthquakes, floods, storms etc.), acts of states, the direct and indirect consequences of wars (declared or undeclared), hostilities, national emergencies, civil commotion and strikes at successful Bidder's premises.

**15. Arbitration & Laws**

Except where otherwise provided for in the contract, all questions and disputes relating to interpretation and application of the provisions of the contract shall be settled mutually within thirty (30 only) days (or such longer period as may be mutually agreed upon) from the date that either party notifies in writing that such dispute or disagreement exists, under the Rules of India Arbitration and Conciliation Act, 1996. The venue of Arbitration shall be specified in the purchase agreement. The jurisdiction of the courts shall be specified in the purchase agreement.

**END OF SECTION III**

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**ANNEXURE A**

**Checklist: Eligibility Criteria for Bidders**

Bidders to indicate whether the following are enclosed by striking out the non-relevant option.

1.	The Demand Draft for Rs.1,00,000/- towards Earnest Money Deposit	Yes/No
2.	Undertaking that the successful bidder agrees to submit the Security Deposit amounting to 5% of the order Value	Yes/No
3.	Undertaking that the successful bidder agrees to give a Performance Bank Guarantee amounting to 10% of the Purchase order Value.	Yes/No
4.	Duly filled Technical Bid with proper seal and signature of authorized person on each page of the bid submitted	Yes/No
5.	Duly filled Financial Bid with Proper Seal and signature of authorized person on each page of the bid submitted	Yes/No
6.	Self Attested copy of Tax Registration Certificate(s) as applicable	Yes/No
7.	Self Attested copy of Sales Tax, Service Tax & other required authorities as applicable	Yes/No
8.	A copy of the Un-priced Financial Bid	Yes/No
9.	Compliance sheet with any deviation	Yes/No

**ANNEXURE – B****(ON STAMP PAPER)****PERFORMANCE BANK GUARANTEE:**

To,

The Director General  
Center for Development of Advanced Computing,  
C-DAC Knowledge Park  
No. 1, Old Madras Road  
Byappanahalli  
Bangalore 560 038.

In consideration of Center for Development of Advanced Computing (hereinafter called the Purchaser) having agreed on the terms and conditions of Order No. : \_\_\_\_\_ dated: \_\_\_\_\_ (hereinafter called the Contract) made between M/s. (Vendor), having its Registered Office at: \_\_\_\_\_, and corporate office at \_\_\_\_\_, (hereinafter called the Contractor) and the Purchaser in connection with supply of \_\_\_\_\_ materials, the Purchaser stipulated in the contract that the balance 10% (Ten Percent only) payment of the purchase price shall be payable to the contractor only against a Bank Guarantee for 10% (Ten percent only) value of order valid till maintenance period contained in the purchase order i.e. 36 months min. from the date of commissioning or min. 40 months from the date of despatch.

We, \_\_\_\_\_(bank name & full address), (hereinafter referred to as the Guarantor), do hereby undertake and agree to indemnify and keep indemnified the Purchaser from time to time to the extent of Rs.\_\_\_\_\_/-(Rs. \_\_\_\_\_ Only) against any cost, charges and expenses suffered by the Purchaser by reasons of any breach or breaches committed by the said Contractor of any of the terms and conditions contained in the contract and the improper performance of the products during the maintenance period and unconditionally pay the amount claimed by the Purchaser on demand and without demur to the aforesaid.

We, (bank name) further agree that the Purchaser shall be the sole judge of and as to whether the said Contractor has committed any breach or breaches of any of the terms and conditions of the said contract and the extent of costs, charges and

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expenses suffered by the Purchaser on account thereof and the decision of the Purchaser that the said contractor has committed such breach or breaches and as to the amount or amounts of costs, charges and expenses suffered by the Purchaser from time to time, shall be final and binding on us.

We, (bank name), further agree that the Guarantee herein contained shall remain in full force and effect during the period that would be taken for the performance of the said contract subject, however, that the Purchaser shall have no claim under this Guarantee after the expiry of the maintenance period as mentioned in the Order No.:\_\_\_\_\_.

The Purchaser shall have the fullest liberty without affecting in any way the liability of the Bank under this Guarantee or Indemnity from time to time to vary any of the terms and conditions of the said Contract or to the extent the time of performance by the said Contractor or to postpone for any time and from time to time any of the powers exercisable by it against the said Contractor and either to enforce or forbear from enforcing any of the terms and conditions governing the said contract or securities available to the Purchaser and the said Bank shall not be released from its responsibilities under these presents by any exercise by the Purchaser to the said contractor or of any other matter or thing whatsoever which under the Law relating to securities would but for this provision have the effect of so releasing the Bank from its such liability.

It shall not be necessary for the Purchaser to proceed against the Contractor before proceeding against the Bank and the Guarantee herein contained shall be enforceable against the Bank, notwithstanding any securities which the Purchaser may have obtained from the Contractor, shall at the time when proceeding are taken against the Bank hereunder be outstanding or unrealized.

We, the said bank, lastly undertake not to revoke this Guarantee during its Currency except with the previous consent of the Purchaser in writing and agree that any change in the constitution of the said contractor or the said bank shall not discharge or liability hereunder.

Notwithstanding anything to the contrary contained hereinbefore our liability under this guarantee is restricted to Rs.\_\_\_\_\_/ - (Rs., in words), our liability under this Guarantee shall remain in force until (date). Unless a demand or claim is made on us in writing, within the said period, that is on or before (date). All rights of the Purchaser under the said Guarantee shall be forfeited and we shall be relieved and discharged from all liabilities.

This Guarantee should be returned to us on expiry.

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Dates this \_\_\_\_\_ day of (month) of \_\_\_\_ (year).

Sd/- (Bankers)

Authorized signatory

With bank seal & full address.

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## **SECTION IV – SCHEDULE OF REQUIREMENTS**

### **Schedule of Requirements:**

#### **PCB Design Tool suite with High Speed SI & PI simulation, EMC analysis, Analog & RF capabilities**

Specifications for PCB Design and Simulation tool suite which must include the following modules:

##### **I. Design Entry : ( Qty: 1 Perpetual License)**

###### **a. Schematic**

- i. Schematic Entry tool to capture design intent for both analog/mixed circuit simulation & PCB design with integrated circuit management
- ii. Easy management of Hierarchical schematic designs
- iii. Easier Cross probing between schematic and PCB Layout tools

###### **b. Library Management**

- i. “A centralized library so that only one version of library needs to be maintained, part table feature to enable multi value parts for single part” or “Allow two users to use the same set of library parts and should have a mechanism to synchronize the parts between two users. It should provide a part table feature to enable multiple value parts for a given Schematic symbol”.
- ii. Easy symbol creation support

###### **c. Should support direct interfacing and is usable with intelligent Design Publisher**

###### **d. Should be interface able or usable along with with the tools in item numbers II to XIII**

##### **II. Schematic : High Speed design support: ( Qty: 1 Perpetual License)**

- a. Topology extraction from Schematic environment : Extraction of topology at schematic level with ideal transmission lines as well as stackup aware lossy transmission lines for signal integrity, cross talk, EMI, timing simulations
- b. Integrated high speed constraint management right from the Schematic stage
- c. High speed signal model assignment like IBIS at schematic level for pre-layout extraction
- d. High speed topology editor built in tool for pre-layout simulation

##### **III. Schematic : Multiple design entry support : ( Qty: 1 Perpetual License)**

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- a. Spread sheet based design entry: The tool should support spread sheet input of components and interconnect data to accommodate very high pin count packages
  - b. Schematic block reuse: Should have capability to create or import schematic block into connectivity capture environment. The connectivity, properties and constraints should also read from schematic
  - c. Easier management of hierarchical designs: Should quickly create and manage hierarchical designs using top-down and bottom up design methodologies. Should support a combination of spreadsheet and schematic blocks in hierarchical design
  - d. Import verilog netlist from existing design
  - e. Quick connectivity creation functions
  - f. Support for functional verification of the design: Support for generating verilog netlist of the design to perform the functional verification of design by simulating the generated netlist in any verilog simulator
  - g. Direct integration with signal integrity environment

**IV. Intelligent Design Publisher option : ( Qty: 1 Perpetual License)**

- a. Creation of intelligent PDFs that enable to view and search the schematic preserving the hierarchy and producing searchable text

**V. Complete Design environment for PCB Layout and Constraint manager for High Speed Designs : ( Qty: 1 Perpetual License)**

**a. PCB Design and Layout**

- i. Intuitive interface to maintain all physical rules and high speed rules
- ii. Cross probing with schematic for individual part selections/list of parts
- iii. Integrated 3D viewer
- iv. Router capability to improve routing around BGAs and other fine-pitched parts
- v. Design Rule Checker to check all types of DRCs

**b. PCB Router**

- i. Router capability to improve routing around BGAs and other fine-pitched parts

**c. High Speed Constraint management**

- i. Easily manage attributes and constraints (layout rules) early in the process so that fewer design iterations are required
- ii. Offer bi-directional communication to integrate the constraints directly with PCB layout and signal integrity analysis
- iii. Handling high speed constraints as an integral part of the environment for both interactive as well as automatic routing
- iv. Common constraint definition environment is shared between schematic capture and layout, allowing the evaluation of critical signals at any stage
- v. Graphical aids for length tuning

**d. Reuse Capability**

- i. “Design reuse capability to store reusable blocks of circuitry including schematic, PCB place and route data in a central library” or “Capability to find and use the previously created reuse blocks of Schematic, PCB place & route data from a central library”.

**e. Should support direct interfacing and is usable with HDI module i.e, item number IX****f. Should be interface able or usable with the tools in item numbers I to III, VI to XIII****g. Output generation**

- i. Output generation at the design level
- ii. Creation of repeatable and consistent manufacturing data sets
- iii. Support for Gerber 274D and 274X, NC Drill/mill, ODB++, Database import/export, DXF import/export, Searchable PDF, GenCAD etc

**VI. PCB: High Speed design support : ( Qty: 1 Perpetual License)**

- a. Native constraint driven design& implementation: constraint driven flow to develop, enter and implement constrains at schematic stage, pre placement stage, post placement stage and post layout stage with single constraint management system across entire stages
- b. True integrated & centralized full constraint management system: Integrated constraint management system which should be integrated with Schematics, Layout, router, Signal Integrity and Waveform viewer with centralized location for all types of constraints namely Physical, Spacing, Electrical, HDI Constraints, DRC and all properties
- c. Tight integration with Signal Integrity Environment: Extraction of electrical topology of board into SI tool. Including via models for SI and cross talk.
- d. Dynamic 3D viewer: PCB tool should have native 3D viewer with filtering options, camera views, graphics control in solid, transparent and wireframe. Ability to view complete design
- e. Incremental ECAD-MCAD co-design: Support ECAD-MCAD Co-design through EDMD standard (IDX). With proper cross-domain change request management, incremental data exchange, graphical preview before accepting changes.
- f. Gerber viewer: Gerber viewing capabilities within or outside the PCB editor to make sure correct Gerber data is generated
- g. Automated topology update and reuse: Should be able to apply constraints developed on topology in SI automatically to large number of nets in one go, tool should have ability to identify appropriate nets & reject incorrect ones for topology application
- h. Dynamic phase control for differential pairs: Support Dynamic Phase Control constraints for differential pairs with real time graphical display showing the line between diff pair where phase mismatch DRC violations with phase mismatch value.

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- i. Differential Phase tuning: Interactive phase tuning adjustment of differential pairs with precision using user defined parameter like bump style, bump length and bump height
  - j. Router with support for shape based routing, 45 degree routing, angled routing taking care of fibre weave effect in high speed boards

**VII. PCB: design planning support ( Qty: 1 Perpetual License)**

- a. Should have tools to plan the pcb layout and route using the abstract data, to perform spatial feasibility analysis
- b. Should be able to generate a topological plan
- c. Should be able to convert the topological plan to traces

**VIII. High Speed Router support ( Qty: 1 Perpetual License)**

- a. Should support constraint driven auto routing, batch routing, user defined routing strategy control
- b. DFM rules driven auto routing
- c. High speed constraints driven auto routing to handle differential pairs routing, timing, crosstalk driven routing
- d. Automatic net shielding to reduce noise on sensitive nets
- e. Layer specific rules support for auto routing

**IX. HDI (High Density Interconnect) support ( Qty: 1 Perpetual License)**

- a. Supports built in HDI features like stacked, staggered microvias
- b. Capable of handling the build-up and microvia structures
- c. Enables localized rules under components to facilitate escape paths

**X. Analog Circuit Simulator Support ( Qty: 1 Perpetual License)**

- a. Supports SPICE modeling
- b. Advanced simulation capabilities such as noise and stress analysis, sensitivity and yield analysis
- c. Various Analyses: covering all aspects of schematic topology performance and accuracy, should cover What if Analysis, AC & DC analysis, parametric Sweep Analysis, Noise Analysis, Monte Carlo analysis and temperature analysis
- d. In built waveform viewer, also allowing multiple waveform viewing
- e. Tight integration with schematic tool
- f. Comprehensive simulation model library covering variety of components such as IGBT, MOSFET, GaAsFET, Non-linear magnetic parts, transmission lines, digital primitives and batteries

- g. Should have model editor
- h. Ability to simulate flat schematics as well as complex multilevel hierarchical schematics

**XI. RF modules support and interfaces ( Qty: 1 Perpetual License)**

- a. Capable of interfacing Agilent ADS interface. It provides an IFF interface also.
- b. Tight integration with ADS RF SCHEMATIC
- c. In-built parameterized RF schematic component library
- d. BI-directional interface with ADS layout with auto-incremental update
- e. Multiple RF design flows: Should support multiple RF design flows include schematic driven RF design, schematic originated RF design & layout driven RF design flow
- f. Tight integration with ADS RF SCHEMATIC: Should allow importing RF circuits from the Agilent ADS design environment to integrate with digital/analog portions of the mixed-signal PCB design. The schematic import should use a wizard-driven flow for symbol creation and schematic update. All ADS parametric RF components should be mapped to schematic RF libraries automatically
- g. Calculator to determine RF parameter: Should have formula-based calculators to determine parameters for RF components
- h. Automatic RF schematic creation: Layout driven RF PCB design flow should automatically generate RF sub-circuit schematic as part of back- annotation in the schematic entry tool

**XII. Signal Integrity and Power Integrity Simulators support for Multi GHz boards including Multi GHz Serial Links simulation ( Qty: 1 No of Perpetual License)****Signal Integrity Analysis Tool**

- a. Supports IBIS models for simulation
- b. Supports IBIS-AMI models for simulation
- c. Supports HSPICE models for simulation
- d. Pre Layout Signal Integrity Analysis
- e. Post Layout signal Integrity Analysis
- f. Visual IBIS editor and Model Support and validation
- g. Tight integration with the schematic capture tool to select a net and launch pre-layout simulation
- h. True integrated & centralized full Constraint Management system
- i. Integrated constraint management system which should be integrated with Schematics, Layout, Signal Integrity and Waveform viewer with centralized location for all types of constraints namely Physical, Spacing, Electrical, HDI Constraints, DRC and all properties

- j. Stack-up aware graphical topology environment: A graphical environment which can perform extraction of electrical views of nets from both pre & post route database, stack-up aware models, capture design constraints to drive the physical design process. Pre-layout should support ideal & lossy transmission line simulations. Single net or differential signal extraction from PCB designer should be possible
- k. Various Simulations : SI tool should cover reflection, crosstalk, pre layout, post layout, IR drop, EMI, Simultaneous switching noise, Bus timing simulations
- l. Crosstalk simulations: Crosstalk simulations by extracting full coupled-line circuits from the layout, walking the victim net and searching within the Geometry Window for aggressors
- m. Crosstalk-Driven Routing: Support automatic or interactive crosstalk-talk driven routing with real time DRCs like (max xtalk & max peak xtalk) which calculate the amount of noise that initially gets coupled over from aggressors
- n. Post-Route Crosstalk Simulation: Support full post-route crosstalk simulation with in-build full coupled-line circuits and stimulate them in the worst-case manner, accounting for reflections, wave addition and cancellation, skin effect and dielectric loss etc
- o. EMI Analysis: Provides EMI simulations which allow to compute differential mode radiated electric field emissions for both far-field EMI and Near field EMI from traces & simulation results include a graphical display of the emission spectrum and a text report summarizing emission details and compliance results
- p. Interconnect characterization field solver: Should have Interconnect extraction field solver implemented with finite element method which combines multiple EM computation modules like static, quasi-TEM and full-wave. Also, should perform the full-wave analysis from DC up to the high frequency of interested by solving Maxwell equations

**Multi GHz Simulation support**

- q. Including loss tangent parameter in the stackup and Zo planning
- r. Accurate modeling of Lossy transmission-line effects, including skin effect and dielectric loss in R-L-G-C pattern
- s. Analyze inter-symbol interference in multi-gigabit signals, including random jitter, eye diagrams and eye masks to define keep out regions
- t. Advanced via modelling
- u. Custom bit and eye mask definition along with PRBS, 8B/10B sequences
- v. Able to define differential vias for differential traces
- w. Integration with H-SPICE(Synopsis)
- x. S-parameter extraction from PCB for selected signals

**Power Integrity Analysis Tool**

- y. IR Drop Analysis: Should have IR drop analysis using attributes Max DC IR Drop, Current Threshold Hold, and Density Threshold Hold .It should have ability to pick

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- one or multiple DC nets(including plane) together to perform the analysis simultaneously
- z. Decoupling Capacitor: Should have Decoupling Capacitor support
  - aa. Adaptive meshing: Power delivery should use rectangular adaptive meshing & the mesh scheme should be adaptive based on the structure of the shape, void, split, slot, or edge
  - bb. Customized color-coded graphical display of analysis: Should have customized color display options (different color legends for different result with method option liner, log, sqrt, exact) for IRDrop analysis such as Display Mesh, Display Current with current flow direction, Display Density, and Display TempRise.
  - cc. 3D EM viewer
  - dd. Full wave Field Solver: Should have Full wave field solver with Optional equivalent model, Debye model, surface roughness support, MoM algorithm with adaptive meshing
  - ee. Resonant Analysis: Should perform a resonant analysis for a plane pair to obtain the S11 curve
  - ff. Pre-Route PI Analysis: Should allow to add virtual noises and virtual vrms for the pre-route PI analysis & allow easily to change stackup or modify shapes
  - gg. Post-Route PI Analysis: Should have post-route PI Network analysis where everything in the real path of the net should be modeled and analyzed, such as shape/void, cline, and via. Coupling effects among shape, void, via, and cline should also be taken into account
  - hh. Model extraction: PI tool allows for extraction of PDN models. These could be extracted as S-parameters, Z-parameters, or Y-parameters and are portable among simulators

**XIII. FPGA-PCB Co-design, System planner & optimization supporting unlimited FPGAs for ASIC prototyping boards ( Qty: 1 No of Perpetual License)**

- a. Fast & easy PCB symbol, component and schematic creation
- b. Tight integration with schematics and PCB layout tools
- c. Bi-directional interface with FPGA vendor tools/constraint files to help designer to optimize , adjust pin assignments to meet functional requirements
- d. Multi FPGA design Optimization supporting unlimited FPGAs
- e. In built DRC to incorporate rules provided by FPGA vendors for pin assignment, reference voltages and terminations

**Other Technical Requirements**

- I. Interface with other standard tools for performing thermal, power integrity, signal integrity, SPICE and RF circuit simulations**
  - a. Synopsys HSPICE

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- b. Agilent ADS
- c. HFSS/SiWave
- d. Flowtherm
- e. Ansys Icepak
- f. SiSoft
- g. Sigrity tools

- II. **Design and Technology kits to take step ahead in design process with templates of pre Layout SI analysis which creates Ready to use environment for standard high Speed Interfaces for eg. DDR3 etc**

**Platform, Training and Support Requirements**

- I. **Maintenance and Support of all the components of the tool to be provided for 3 years**
- II. **Training covering all tools for a group of 10 people, 5 times ( total 25 days) spread over first two years of maintenance period as per vendor and CDAC's mutual date of convenience**
- III. **Support for 64 bit multi core processor platforms, under Windows/ Linux Environments**
- IV. **Vendor should quote for Floating License Option for each of the above tools.**
- V. **Should support Re-hosting the license server in case of any unexpected crash of machine hosting license server.**